# CLAIMS

1. A method of forming a MOSFET device comprising:

providing a substrate;

forming on said substrate a relaxed SiGe layer having a Ge content between 0.51 and 0.80; and

depositing on said relaxed SiGe layer a $\varepsilon$-Si layer.

2. The method of claim 1, wherein said $\varepsilon$-Si layer is sized approximately at 45Å.

3. The method of claim 1 further comprising planarizing said SiGe layer.

4. The method of claim 3, wherein said planarizing comprises CMP.

5. The method of claim 1, wherein said MOSFET device comprises a hole mobility enhancement that increases with effective vertical field.

6. The method of claim 5, wherein said hole mobility enhancement saturates approximately around 2.5.

7. The method of claim 1, wherein said $\varepsilon$-Si layer shifts the hole wave function away from the surface of said $\varepsilon$-Si layer.

8. The method of claim 1, wherein said substrate comprises a crystalline Si substrate.

9. The method of claim 1, wherein said substrate comprises a crystalline Si substrate and a relaxed SiGe graded layer.

10. The method of claim 1, wherein said substrate comprises a crystalline substrate and an insulating layer.

11. The method of claim 10, wherein said insulator layer comprises an oxide.

12. The method of claim 1, wherein said MOSFET device comprises a PMOS device.

13. The method claim 12, wherein said MOSFET device comprises a NMOS device.

14. The method claim 13, wherein said PMOS and NMOS devices form a CMOS device.

15. The method of claim 1, wherein said relaxed SiGe layer comprises a selective portion having a Ge content between 0.7 and 0.75.

16. A method of forming a MOSFET device comprising:

providing a substrate;

forming on said substrate a relaxed SiGe layer having a Ge content between 0.51 and 0.80; and

forming on said relaxed SiGe layer a digital alloy structure that comprises alternating layers of ε-Si and SiGe having a Ge content between 0.51 and 1, wherein said mobility enhancement of said device is constant.

17. The method of claim 16, wherein said alternating layers of SiGe and ε-Si are sized approximately at 10Å.

18. The method of claim 16 further comprising planarizing said relaxed SiGe layer.

19. The method of claim 18, wherein said planarizing comprises CMP.

20. The method of claim 16, wherein said ε-Si layer shifts the hole wave function away from the surface of said ε-Si layer.

21. The method of claim 16, wherein said substrate comprises a crystalline Si substrate.

22. The method of claim 16, wherein said substrate comprises a crystalline Si substrate and a relaxed SiGe graded layer.

23. The method of claim 16, wherein said substrate comprises a crystalline substrate and an insulating layer.

24. The method of claim 23, wherein said insulator layer comprises an oxide.

25. The method of claim 16, wherein said MOSFET device comprises a PMOS device.

26. The method claim 25, wherein said MOSFET device comprises a NMOS device.

27. The method claim 26, wherein said PMOS and NMOS devices form a CMOS device.

28. The method of claim 16, wherein said relaxed SiGe layer comprises a selective portion having a Ge content between 0.7 and 0.75.

29. A method of forming a MOSFET device comprising:

providing a substrate;

forming on said substrate a relaxed SiGe layer having a Ge content between 0.51 and 0.80; and

depositing on said relaxed SiGe layer a ε-Si layer so that hole mobility enhancement increases with effective vertical field.

30. The method of claim 29, wherein said ε-Si layer is sized approximately at 45Å.

31. The method of claim 29 further comprising planarizing said relaxed SiGe layer.

32. The method of claim 31, wherein said planarizing comprises CMP.

33. The method of claim 29, wherein said MOSFET device comprises a hole mobility enhancement that increases with effective vertical field.

34. The method of claim 29, wherein said hole mobility enhancement saturates approximately around 2.5.

35. The method of claim 29, wherein said ε-Si layer shifts the hole wave function away from the surface of said ε-Si layer.

36. The method of claim 29, wherein said substrate comprises a crystalline Si substrate.

37. The method of claim 29, wherein said substrate comprises a crystalline Si substrate and a relaxed SiGe graded layer.

38. The method of claim 29, wherein said substrate comprises a crystalline substrate and an insulating layer.

39. The method of claim 38, wherein said insulator layer comprises an oxide.

40. The method of claim 29, wherein said MOSFET device comprises a PMOS device.

41. The method of claim 40, wherein said MOSFET device comprises a NMOS device.

42. The method claim 41, wherein said PMOS and NMOS devices form a CMOS device.

43. A MOSFET device comprising:

a substrate;

a relaxed SiGe layer that is formed on said substrate having a Ge content between 0.51 and 0.80; and

a ε-Si layer that is deposited on said relaxed SiGe layer.

44. The MOSFET device of claim 43, wherein said ε-Si layer is sized approximately at 45Å.

45. The MOSFET device of claim 43, wherein said relaxed SiGe layer is planarized.

46. The MOSFET device of claim 43 further comprising a hole mobility enhancement that increases with effective vertical field.

47. The MOSFET device of claim 46, wherein said hole mobility enhancement saturates approximately around 2.5.

48. The MOSFET device of claim 43, wherein said ε-Si layer shifts the hole wave function away from the surface of said ε-Si layer.

49. The MOSFET device of claim 43, wherein said substrate comprises a crystalline Si substrate.

50. The MOSFET device of claim 43, wherein said substrate comprises a crystalline Si substrate and a relaxed SiGe graded layer.

51. The MOSFET device of claim 43, wherein said substrate comprises a crystalline substrate and an insulating layer.

52. The MOSFET device of claim 51, wherein said insulator layer comprises an oxide.

53. The MOSFET device of claim 43 further comprising a PMOS device.

54. The MOSFET device of claim 53 further comprising a NMOS device.

55. The MOSFET device of claim 54, wherein said PMOS and NMOS devices form a CMOS device.

56. The MOSFET device of claim 43, wherein said relaxed SiGe layer comprises a selective portion having a Ge content between 0.7 and 0.75.

57. A MOSFET device comprising:

a substrate;

a relaxed SiGe layer that is formed on said substrate having a Ge content between 0.51 and 0.80; and

a digital alloy structure that is formed on said relaxed SiGe layer comprising alternating layers of $\varepsilon$-Si and SiGe having a Ge content between 0.51 and 1, wherein said mobility enhancement of said device is constant.

58. The MOSFET device of claim 57, wherein said alternating layers of SiGe and $\varepsilon$-Si is sized approximately at 45Å.

59. The MOSFET device of claim 57, wherein said relaxed SiGe layer is planarized.

60. The MOSFET device of claim 57, wherein said $\varepsilon$-Si layer shifts the hole wave function away from the surface of said $\varepsilon$-Si layer.

61. The MOSFET device of claim 57, wherein said substrate comprises a crystalline Si substrate.

62. The MOSFET device of claim 57, wherein said substrate comprises a crystalline Si substrate and a relaxed SiGe graded layer.

63. The MOSFET device of claim 57, wherein said substrate comprises a crystalline substrate and an insulating layer.

64. The MOSFET device of claim 63, wherein said insulator layer comprises an oxide.

65. The MOSFET device of claim 57 further comprising a PMOS device.

66. The MOSFET device claim 65 further comprising a NMOS device.

67. The MOSFET device claim 66, wherein said PMOS and NMOS devices form a CMOS device.

68. The MOSFET device of claim 57, wherein said relaxed SiGe layer comprises a selective portion having a Ge content between 0.7 and 0.75.

69. A MOSFET device comprising:

a substrate;

a relaxed SiGe layer that is formed on said substrate having a Ge content between 0.51 and 0.80; and

a ε-Si layer that is deposited on said relaxed SiGe layer so that hole mobility enhancement increases with effective vertical field.

70. The MOSFET device of claim 69, wherein said ε-Si layer is sized approximately at 45Å.

71. The MOSFET device of claim 69, wherein said relaxed SiGe layer is planarized.

72. The MOSFET device of claim 69, wherein said MOSFET device comprises a hole mobility enhancement that increases with effective vertical field.

73. The MOSFET device of claim 72, wherein said hole mobility enhancement saturates approximately around 2.5.

74. The MOSFET device of claim 69, wherein said ε-Si layer shifts the hole wave function away from the surface of said ε-Si layer.

75. The MOSFET device of claim 69, wherein said substrate comprises a crystalline Si substrate.

76. The MOSFET device of claim 69, wherein said substrate comprises a crystalline Si substrate and a relaxed SiGe graded layer.

77. The MOSFET device of claim 69, wherein said substrate comprises a crystalline substrate and an insulating layer.

78. The MOSFET device of claim 77, wherein said insulator layer comprises an oxide.

79. The MOSFET device of claim 69 further comprising a PMOS device.

80. The MOSFET device of claim 79 further comprising a NMOS device.

81. The MOSFET device claim 80, wherein said PMOS and NMOS devices form a CMOS device.